Kongunadu College of Engineering and Technology
(Autonomous)
Affiliated to Anna University, Chennai
M.E. Applied Electronics
Regulations:KNCET-PGR2020
Choice Based Credit System
I to IV Semesters Curricula & Syllabi

Semester I							
S.No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
Theory							
1	20AEMA101	Applied Mathematics for Electronics Engineers	FC	4	0	0	4
2	20AE101	Advanced Digital System Design	PCC	3	0	0	3
3	20AE102	Advanced Digital Signal Processing	PCC	3	2	0	4
4	20AE103	Embedded System Design	PCC	3	0	0	3
5	20AE104	Sensors, Actuators and Interface Electronics	PCC	3	0	0	3
6		Professional Elective I	PEC	3	0	0	3
Practicals							
7	20AE101L	Electronic System Design Laboratory I	PCC	0	0	4	2
			Total	**19**	**2**	**4**	**22**

Semester II							
S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
Theory							
1	20AE201	Soft Computing and Optimization Techniques	PCC	3	0	0	3
2	20AE202	ASIC and FPGA Design	PCC	3	0	0	3
3	20AE203	Hardware-Software Co-Design	PCC	3	0	0	3
4	20AE204	Digital Image Processing	PCC	3	0	0	3
5		Professional Elective II	PEC	3	0	0	3
6		Professional Elective III	PEC	3	0	0	3
Practicals							
7	20AE201L	Electronic System Design Laboratory II	PCC	0	0	4	2
8	20AEEEC201	Term Paper Writing and Seminar	EEC	0	0	2	1
			Total	**18**	**0**	**6**	**21**

CHAIRMAN
BOS/ECE

Semester III							
S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
Theory							
1	20AE301	Advanced Microprocessors and Microcontrollers Architectures	PCC	3	0	0	3
2	PG20MC002	Universal Human Values 2: Understanding Harmony	HSC	3	0	0	3
3		Professional Elective IV	PEC	3	0	0	3
4		Professional Elective V	PEC	3	0	0	3
Practicals							
7	20AEEEC301	Project Work Phase I	EEC	0	0	12	6
			Total	**12**	**0**	**12**	**18**

Semester IV							
S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
Practicals							
7	20AEEEC401	Project Work Phase II	EEC	0	0	24	12
			Total	**0**	**0**	**24**	**12**

CHAIRMAN
BOS/ECE

Professional Elective Course (PEC)

Semester- I
Elective I

S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
1	20AEPE101	Digital Control Engineering	PEC	3	0	0	3
2	20AEPE102	Computer Architecture and Parallel Processing	PEC	3	0	0	3
3	20AEPE103	CAD for VLSI Circuits	PEC	3	0	0	3
4	20AEPE104	Electromagnetic Interference and Compatibility	PEC	3	0	0	3

Semester- II
Elective II

S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
1	20AEPE201	VLSI Design Techniques	PEC	3	0	0	3
2	20AEPE202	Nano Electronics	PEC	3	0	0	3
3	20AEPE203	Wireless Adhoc and Sensor Networks	PEC	3	0	0	3
4	20AEPE204	High Performance Networks	PEC	3	0	0	3

Semester- II
Elective III

S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
1	20AEPE205	DSP Processor Architecture and Programming	PEC	3	0	0	3
2	20AEPE206	RF System Design	PEC	3	0	0	3
3	20AEPE207	Speech and Audio Signal Processing	PEC	3	0	0	3
4	20AEPE208	Solid State Device Modeling and Simulation	PEC	3	0	0	3

CHAIRMAN
BOS/ECE

Semester- III
Elective IV

S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
1	20AEPE301	Internet of Things	PEC	3	0	0	3
2	20AEPE302	System on Chip Design	PEC	3	0	0	3
3	20AEPE303	Robotics	PEC	3	0	0	3
4	20AEPE304	Optical Networks	PEC	3	0	0	3

Semester- III
Elective V

S. No	Course Code	Course Title	Course Category	No of Hours/Week			Credit
				L	T	P	
1	20AEPE305	Signal Integrity for High Speed Design	PEC	3	0	0	3
2	20AEPE306	MEMS and NEMS	PEC	3	0	0	3
3	20AEPE307	Secure Computing Systems	PEC	3	0	0	3
4	20AEPE308	Pattern Recognition	PEC	3	0	0	3

CHAIRMAN
BOS/ECE

KONGUNADU COLLEGE OF ENGINEERING AND TECHNOLOGY
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To create highly skilled, proficient and excellent Electronics and Communication Engineers having professional ethics, passion and competence to adapt to the latest transformations in technology.

MISSION

- Promoting quality teaching and effective learning to face the global challenges.
- Enriching professionals of high caliber to excel in their careers through students' overall development.
- Promoting education that imparts multidisciplinary design approaches, innovation and creativity.

PROGRAM EDUCATIONAL OBJECTIVES (PEO):

- **PEO I:** Graduates shall exhibit the skills and knowledge required to design, develop and implement solutions for real life problems..
- **PEO II:** Graduates shall excel in professional career, higher education and research
- **PEO III:** Graduates shall demonstrate professionalism, entrepreneurship, ethical behavior, communication skills and collaborative team work to adapt to the emerging trends by engaging in lifelong learning.

PROGRAM OUTCOMES(PO):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

CHAIRMAN
BOS/ECE

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life Long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

POGRAM SPECIFIC OUTCOMES (PSO's):

- **PSO1:** Students shall have skills and knowledge to work and design on PCB, analog and digital systems, adhoc and sensor networks, embedded and communication systems
- **PSO2:** Students are able to perform and design in the simulation tools and IoT related modules.

CHAIRMAN
BOS/ECE

20AEMA101 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS **L T P C**

4 0 0 4

OBJECTIVES:

The Student should be made to:

- Study and understand the concepts of Fuzzy logic techniques, classical logic, multivalued logic and fuzzy quantifiers and its applications
- Develop the use of matrix algebra and its theory of techniques this is needed by engineers for practical applications
- Study and understand the concepts of probability and random variable of the various functions
- Study and understand the concepts of Dynamic programming, Principle of optimality, Forward and backward recursion and its applications
- Be exposed to basic characteristic features of a queuing system and acquire skills in analyzing queuing models

UNIT I FUZZY LOGIC **12**

Classical logic - Multivalued logics - Fuzzy propositions - Fuzzy quantifiers.

UNIT II MATRIX THEORY **12**

Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT III PROBABILITY AND RANDOM VARIABLES **12**

Probability - Axioms of probability - Conditional probability – Baye's theorem - Random variables - Probability function - Moments - Moment generating functions and their properties - Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions - Function of a Random variable.

UNIT IV DYNAMIC PROGRAMMING **12**

Dynamic programming - Principle of optimality - Forward and backward recursion - Applications of dynamic programming - Problem of dimensionality.

UNIT V QUEUEING MODELS **12**

Poisson Process - Markovian queues - Single and multi server models - Littles formula - Machine interference model - Steady state analysis - Self service queue.

TOTAL: 60 PERIODS

CHAIRMAN
BoS (Maths)

CHAIRMAN
BoS (ECE)

OUTCOMES:

On successful completion of this course, the students will be able to,

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.
- Apply various methods in matrix theory to solve system of linear equations.
- Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
- Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
- Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.

REFERENCES:

1. Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.
2. George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.
3. Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014.
4. Johnson, R.A., Miller, I and Freund J., "Miller and Freunds "Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.
5. Taha, H.A., "Operations Research: An Introduction", 9 th Edition, Pearson Education, Asia, New Delhi, 2016.

CHAIRMAN
BoS (Maths)

CHAIRMAN
BoS (ECE)

20AE101 **ADVANCED DIGITAL SYSTEM DESIGN** L T P C
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Introduce methods to analyze and design synchronous sequential circuits.
- Introduce methods to analyze and design asynchronous sequential circuits.
- Diagnosis the different fault algorithms and testability algorithms
- Implement various synchronous design using programmable devices
- Introduce design and implementation of digital circuits using programming tools.

.UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits- ASM chart and realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit - flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards - data synchronizers - mixed operating mode asynchronous circuits - designing vending machine controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method - Boolean difference method-D algorithm - Tolerance techniques - The compact algorithm - Fault in PLA - Test generation-DFT schemes - Built in self test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families - Designing a synchronous sequential circuit using PLA/PAL - Realization of finite state machine using PLD - FPGA - Xilinx FPGA-Xilinx 4000.

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL - Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL - HDL Based Synthesis - Synthesis of Finite State Machines- structural modeling - compilation and simulation of Verilog code -Test bench - Realization of combinational and sequential circuits using Verilog - Registers - counters - sequential machine - serial adder - Multiplier- Divider - Design of simple microprocessor.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Diagnosis the different fault algorithms and testability algorithms

CHAIRMAN
BoS /ECE

- Implement various synchronous design using programmable devices
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES :

1. Charles H.Roth Jr, "Fundamentals of Logic Design", Thomson Learning 2004
2. M.D.Ciletti, "Modeling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice Hall, 1999.
3. M.G.Arnold, "Verilog Digital - Computer Design", Prentice Hall (PTR), 1999.
4. Nripendra N Biswas, "Logic Design Theory" Prentice Hall of India,2001
5. Parag K.Lala "Digital system Design using PLD" B S Publications,2003
6. Parag K.Lala. "Fault Tolerant and Fault Testable Hardware Design", B S Publications,2002
7. S. Palnitkar , "Verilog HDL - A Guide to Digital Design and Synthesis", Pearson , 2003.

CHAIRMAN
BoS /ECE

20AE102 ADVANCED DIGITAL SIGNAL PROCESSING

L	T	P	C
3	2	0	4

OBJECTIVES:

The Student should be made to:

- Study the comprehends mathematical description and modeling of discrete time random signals.
- Learn the conversant with important theorems and random signal processing algorithms.
- Acquire the learns relevant figures of merit such as power, energy, bias and consistency.
- Understand the familiar with estimation, prediction, filtering, multirate concepts and techniques.
- Analysis the different multi rate signal processing

UNIT I DISCRETE RANDOM SIGNAL PROCESSING **9+6**

Wide sense stationary process - Ergodic process - Mean - Variance - Auto-correlation and Auto-correlation matrix - Properties - Weiner Khitchine relation - Power spectral density - filtering random process, Spectral Factorization Theorem-Finite Data records, Simulation of uniformly distributed/Gaussian distributed white noise - Simulation of Sine wave mixed with Additive White Gaussian Noise.

UNIT II SPECTRUM ESTIMATION **9+6**

Bias and Consistency of estimators - Non-Parametric methods - Correlation method - Co-variance estimator - Performance analysis of estimators - Unbiased consistent estimators - Periodogram estimator - Barlett spectrum estimation - Welch estimation.

UNIT III LINEAR ESTIMATION AND PREDICTION **9+6**

Model based approach - AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walker method - Maximum likelihood criterion - Efficiency of estimator - Least mean squared error criterion - Wiener filter - Discrete Wiener Hoff equations - Mean square error.

UNIT IV ADAPTIVE FILTERS **9+6**

Recursive estimators - Kalman filter - Linear prediction - Forward prediction and Backward prediction, Prediction error - Whitening filter, Inverse filter - Levinson recursion, Lattice realization, Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT V MULTIRATE DIGITAL SIGNAL PROCESSING **9+6**

FIR Adaptive filters - Newton's steepest descent method - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters - Exponentially weighted RLS - Sliding window RLS - Simplified IIR LMS Adaptive filter.

TOTAL: 45+30:75 PERIODS

CHAIRMAN
BoS /ECE

OUTCOMES:

On successful completion of this course, the students will be able to,

- Study the Formulate time domain and frequency domain description of Wide Sense Stationary process in terms of matrix algebra and relate to linear algebra concepts.
- Learn the W-K theorem, spectral factorization theorem, spectrum estimation, bias and consistency of estimators.
- Acquire the different wiener filtering, LMS algorithms, Levinson recursion algorithm, applications of adaptive filters
- Understand the decimation, interpolation, Sampling rate conversion, Applications of multirate signal processing
- Analyze the different multi rate signal processing.

REFERENCES :

1. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of
2. India, New Delhi, 2005.
3. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 2006.
4. P. P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, 1992.
5. S. Kay, "Modern spectrum Estimation theory and application", Prentice Hall, Englehood Cliffs, NJ1988.
6. Simon Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs, NJ1986.
7. Sophoncles J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000.

CHAIRMAN
BoS /ECE

20AE103 **EMBEDDED SYSTEM DESIGN** L T P C
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Provide the basics of Embedded system design challenges
- Understand the design concept of general and single purpose processor
- Analyze the fundamentals of basic protocol concepts of bus structures.
- Be familiar with the knowledge on finite state machine model.
- Make in depth knowledge in software development tools and RTOS.

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges - Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmers view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing - I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols - PCI and ARM Bus, Wireless Protocols - IrDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

Compilation Process - Libraries - Porting kernels - C extensions for embedded systems - emulation and debugging techniques - RTOS - System design using RTOS.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Gain knowledge on basics of embedded design challenges, design metrics and design methodologies
- Understand the architecture of single purpose processor with the help of architectural components.
- Design and implement various types of wireless protocols on the embedded control system.
- Analyze the finite-state machine with data path Model on sequential circuits.
- Implement RTOS based system for real time applications.

CHAIRMAN
BoS /ECE

REFERENCES:

1. Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.
2. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.
3. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.
4. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.

CHAIRMAN
BoS /ECE

20AE104 SENSORS, ACTUATORS AND INTERFACE ELECTRONICS **L T P C**
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand static and dynamic characteristics of measurement systems.
- Applying various types of sensors for different applications
- Analyzing different typess of actuators and their usage.
- Understanding the concept of Signal conditioning and self-generating motors
- Designing State-of-the-art digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS **9**

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS **9**

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to the LVDT.

UNIT III SELF-GENERATING SENSORS **9**

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS **9**

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS **9**

Digital sensors: position encoders, variable frequency sensors - quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.

TOTAL: 45 PERIODS

CHAIRMAN
BoS /ECE

OUTCOMES:

On successful completion of this course, the students will be able to,

- Understand the Measurements systems
- Evaluate digital sensors and semiconductor device sensors
- Utilize the Self-generating sensors
- Compare Actuators according to their applications
- Design State-of-the-art digital and semiconductor sensors

REFERENCES :

1. Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2006.
2. D. Johnson, "Process Control Instrumentation Technology", John Wiley and Sons.
3. D.Patranabis, "Sensors and Transducers", TMH 2003.
4. E.O. Doeblin, "Measurement System : Applications and Design", McGraw Hill publications
5. Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.
6. Herman K.P. Neubrat, "Instrument Transducers - An Introduction to Their Performance and Design", Oxford University Press.
7. Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.
8. Jon Wilson , "Sensor Technology Handbook", Newne 2004.
9. Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
10. Ramon Pallreny, John G. Webster, "Sensors and Signal Conditioning", 2nd edition, John Wiley and Sons, 2000.
11. Sensors and Actuators: Control System Instrumentation, Clarence W. de Silva CRC Press,2007.

CHAIRMAN
BoS /ECE

20AE101L ELECTRONIC SYSTEM DESIGN LABORATORY I

L	T	P	C
0	0	4	2

OBJECTIVES:

The Student should be made to:

- Study the different interfaces techniques
- Learn asynchronous and clocked synchronous sequential circuits
- Understand the concept of built in self test and fault diagnosis
- Learn built in self and fault diagnosis
- Design and analysis of real time signal processing system

LIST OF THE EXPERIMENTS

1. System design using PIC, MSP430, 51 Microcontroller and 16- bit Microprocessor - 8086.
2. Study of different interfaces (using embedded microcontroller)
3. Implementation of Adaptive Filters and multistage multirate system in DSP Processor
4. Simulation of QMF using Simulation Packages
5. Analysis of Asynchronous and clocked synchronous sequential circuits
6. Built in self test and fault diagnosis
7. Sensor design using simulation tools
8. Design and analysis of real time signal processing system - Data acquisition and signal processing

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Apply PIC, MSP430, 8051 Microcontroller and 8086 for system design
- Study and Simulate QMF
- Design sensor using simulation tools
- Analyze the asynchronous and clocked synchronous sequential circuits
- Design and analyze of real time signal processing system

CHAIRMAN
BoS /ECE

20AE201 SOFT COMPUTING AND OPTIMIZATION TECHNIQUES

L	T	P	C
3	0	0	3

OBJECTIVES:

The Student should be made to:

- Familiarizes with the design of various neural networks.
- Understand the concept of fuzzy logic.
- Gain insight onto Neuro Fuzzy modeling and control.
- Gain knowledge in conventional optimization techniques.
- Understand the various evolutionary optimization techniques.

UNIT I NEURAL NETWORKS **9**

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks - Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks - Self Organizing map , Adaptive Resonance Architectures, Hopfield network.

UNIT II FUZZY LOGIC **9**

Fuzzy Sets - Operations on Fuzzy Sets - Fuzzy Relations - Membership Functions-Fuzzy Rules and Fuzzy Reasoning - Fuzzy Inference Systems - Fuzzy Expert Systems - Fuzzy Decision Making.

UNIT III NEURO-FUZZY MODELING **9**

Adaptive Neuro-Fuzzy Inference Systems - Coactive Neuro-Fuzzy Modeling - Classification and Regression Trees - Data Clustering Algorithms - Rule base Structure Identification - Neuro-Fuzzy Control - Case Studies.

UNIT IV CONVENTIONAL OPTIMIZATION TECHNIQUES **9**

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newtons Method, Marquardt Method, Constrained optimization -sequential linear programming, Interior penalty function method, external penalty function method.

UNIT V EVOLUTIONARY OPTIMIZATION TECHNIQUES **9**

Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Implement machine learning through Neural networks.
- Develop a Fuzzy expert system.
- Model Neuro Fuzzy system for clustering and classification.
- Use the optimization techniques to solve the real world problems.
- Use the genetic algorithm to solve the real time problems.

CHAIRMAN
BoS /ECE

REFERENCES :

1. David E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Addison wesley, 2009.
2. George J. Klir and Bo Yuan, "Fuzzy Sets and Fuzzy Logic-Theory and Applications", Prentice Hall, 1995.
3. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques", Pearson Edn., 2003.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, "Neuro-Fuzzy and Soft Computing", Prentice-Hall of India, 2003.
5. Mitchell Melanie, "An Introduction to Genetic Algorithm", Prentice Hall, 1998.
6. Simon Haykins, "Neural Networks: A Comprehensive Foundation", Prentice Hall International Inc, 1999.
7. Singiresu S. Rao, "Engineering optimization Theory and practice", John Wiley & sons, inc, 4th Edition, 2009
8. Timothy J.Ross, "Fuzzy Logic with Engineering Applications", McGraw-Hill, 1997.
9. Venkata Rao, Vimal J. Savsani, "Mechanical Design Optimization Using Advanced Optimization Techniques", springer 2012.

CHAIRMAN
BoS /ECE

20AE202	ASIC AND FPGA DESIGN	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Study the design flow of different types of ASIC.
- Gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC.
- Familiarize the different types of programming technologies and logic devices
- Learn the architecture of different types of FPGA.
- Know the system on chip design and the performance.

UNIT I OVERVIEW OF ASIC AND PLD 9

Types of ASICs - Design flow - CAD tools used in ASIC Design - Programming Technologies: Antifuse - static RAM - EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs - PLA -PAL. Gate Arrays - CPLDs and FPGAs.

UNIT II ASIC PHYSICAL DESIGN 9

System partition -partitioning - partitioning methods - interconnect delay models and measurement of delay - floor planning - placement - Routing: global routing - detailed routing - special routing - circuit extraction - DRC.

UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV FIELD PROGRAMMABLE GATE ARRAYS 9

FPGA Design: FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

UNIT V SOC DESIGN 9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Design different types of ASIC models.
- Implement the physical design for different models.
- Analyze the synthesis, Simulation and testing of systems.
- Discuss the implementation of FPGA in SOC.
- Apply different high performance algorithms in ASICs.

CHAIRMAN
BoS /ECE

REFERENCES :

1. David E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Addison wesley, 2009.
2. George J. Klir and Bo Yuan, "Fuzzy Sets and Fuzzy Logic-Theory and Applications", Prentice Hall, 1995.
3. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques", Pearson Edn., 2003.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, "Neuro-Fuzzy and Soft Computing", Prentice-Hall of India, 2003.
5. Mitchell Melanie, "An Introduction to Genetic Algorithm", Prentice Hall, 1998.
6. Simon Haykins, "Neural Networks: A Comprehensive Foundation", Prentice Hall International Inc, 1999.
7. Singiresu S. Rao, "Engineering optimization Theory and practice", John Wiley & sons, inc, 4th Edition, 2009
8. Timothy J.Ross, "Fuzzy Logic with Engineering Applications", McGraw-Hill, 1997.
9. Venkata Rao, Vimal J. Savsani, "Mechanical Design Optimization Using Advanced Optimization Techniques", springer 2012.

CHAIRMAN
BoS /ECE

20AE203 **HARDWARE - SOFTWARE CO-DESIGN** L T P C
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Acquire the knowledge about system specification and modeling.
- Learn the formulation of partitioning
- Compare the software and hardware co synthesis.
- Study the different technical aspects about prototyping and emulation.
- Know the design specification and verification methods.

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE / SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification' Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Gain knowledge about co design modeling.
- Identify the partitioning design problems and issues
- To compare hardware / software co-synthesis.

CHAIRMAN
BoS /ECE

REFERENCES :

1. David A.Hodges, "Analysis and Design of Digital Integrated Circuits", (3/e), MGH 2004
2. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley, 1999
3. Jan. M. Rabaey et al, "Digital Integrated Circuit Design Perspective" (2/e), PHI 2003
4. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2003
5. J. Old Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley& Sons, Newyork.
6. P.K.Chan & S. Mourad, "Digital Design using Field Programmable Gate Array", Prentice Hall.
7. Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures System on Chip Interconnect", Elsevier, 2008
8. S.Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Pub.
9. S.Brown,R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array", Kluwer Pub.
10. Richard FJinder , "Engineering Digital Design", Academic press.

CHAIRMAN
BoS /ECE

20AE204 **DIGITAL IMAGE PROCESSING** L T P C
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand fundamentals of digital image processing
- Learn different image transforms and its functions
- Study the concept of segmentation in image processing.
- Understand the image enhancement technique and colour image processing.
- Know the different types of compression algorithms

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III SEGMENTATION OF GRAY LEVEL IMAGES 9

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

UNIT V IMAGE COMPRESSION 9

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Gain knowledge in image processing fundamentals.
- Discuss about the different types of image transformation techniques.
- Discuss image enhancement techniques and know the colour image processing methods.
- Understand the different types enhancement techniques and its performances.
- Compare image compression schemes based on the performances.

CHAIRMAN
BoS /ECE

- To assess prototyping and emulation techniques
- To formulate the design specification and validate its functionality by simulation

REFERENCES:

1. Giovanni De Micheli , Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design", Kaufmann Publishers, 2001.
2. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Pub, 1997.
3. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.

CHAIRMAN
BoS /ECE

20AE201L **ELECTRONIC SYSTEM DESIGN LABORATORY II** **L T P C**
0 0 4 2

OBJECTIVES:

The Student should be made to:

- Study of 32 bit ARM7 microcontroller RTOS and its application
- Understand testing RTOS environment and system programming
- Learn wireless network design using embedded systems
- Learn System design using ASIC
- Know use of Verilog and VHDL in sequential digital system modeling

LIST OF THE EXPERIMENTS

1. Study of 32 bit ARM7 microcontroller RTOS and its application
2. Testing RTOS environment and system programming
3. Designing of wireless network using embedded systems
4. Implementation of ARM with FPGA
5. Design and Implementation of ALU in FPGA using VHDL and Verilog
6. Modeling of Sequential Digital system using Verilog and VHDL
7. Flash controller programming - data flash with erase, verify and fusing
8. System design using ASIC
9. Design, simulation and analysis of signal integrity

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Utilize ARM with FPGA
- Demonstrate design of ALU in FPGA using VHDL and Verilog
- Assess flash controller programming - data flash with erase, verify and fusing
- Design using ASIC
- Explain design, simulation and analysis of signal integrity.

CHAIRMAN
BoS /ECE

20AEEEC201 **TERM PAPER WRITING AND SEMINAR** **L T P C**
0 0 2 1

OBJECTIVES:

The Student should be made to:

- Develop their scientific and technical reading and writing skills that they needs
- Understand and construct research articles.
- Obtain information from a variety of sources (i.e., Journals, dictionaries, reference books)
- Place it in logically developed ideas.

THE WORK INVOLVES THE FOLLOWING STEPS:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing
6. each paper.
7. Preparing a working outline
8. Linking the papers and preparing a draft of the paper.
9. Preparing conclusions based on the reading of all the papers.
10. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.

ACTIVITIES TO BE CARRIED OUT

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	3% Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd week	3% (the selected information must be area specific and of international and national standard)

CHAIRMAN
BoS /ECE

Collection of Journal papers in the topic in the context of the objective collect 20 & then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to:Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour first or foundational papers in the field (as indicated in other people? survey paper), • Favour more recent papers, Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/ categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered.	4th week	6% (the list of standard papers and reason for selection)
Reading and notes for first 5 papers	• Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion?	5th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

CHAIRMAN
BoS /ECE

	• What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations / issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next 5 papers	Repeat Reading Paper Process	6th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	8% (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	6% (Clarity, purpose and conclusion) 6% Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	5% (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11th week	10% (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	5% (conclusions clarity and your ideas)

CHAIRMAN
BoS /ECE

Final Draft	Complete the final draft of your paper	13th week	10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	10% (based on presentation and Viva- voce)

TOTAL: 30 PERIODS

CHAIRMAN
BoS /ECE

20AE301	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES	L T P C 3 0 0 3

OBJECTIVES:

The students should be made to

- Familiarize about the features, specification and features of modern microprocessors.
- Gain knowledge about the architecture of Intel 32 and 64 bit microprocessors and salient features associated with them.
- Familiarize about the features, specification and features of modern microcontrollers.
- Gain knowledge about the 32 bit microcontrollers based on ARM and PIC32 architectures
- Learn about ARM - M3 architecture and its salient features

UNIT I FEATURES OF MODERN MICROPROCESSORS 9

Evolution of microprocessors - Data and Address buses - clock speed - memory interface - multi-core architectures - cache memory hierarchy - operating modes - super scaler execution - dynamic execution - over clocking - integrated graphics processing - performance benchmarks.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURES 9

Introduction to IA 32 bit architecture - Intel Pentium Processors family tree - Memory Management - Branch prediction logic - Superscalar architecture - Hyper threading technology - 64 bit extension technology - Intel 64 bit architecture - Intel Core processor family tree - Turbo boost technology - Smart cache - features of Nehalem microarchitecture.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

RISC architecture merits and demerits - The programmer's model of ARM Architecture - 3-stage pipeline ARM organization - 3-stage pipeline ARM organization - ARM instruction execution - Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles).

UNIT IV FEATURES OF MODERN MICROPROCESSORS 9

Introduction to microcontrollers - microcontroller vs microprocessors - microcontroller architecture - Processor Core - Memory interfaces- Communication interfaces (SPI,I2C, USB and CAN) - ADC - PWM - Watchdog timers - Interrupts - Debugging interfaces.

UNIT V HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES 9

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers - Thumb 2 instruction technology - Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling - Applications of Cotex-M3 architecture.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Explain the features and important specifications of modern microprocessors
- Identify the salient features CISC microprocessors based on IA-32 bit and IA-64 bit architectures

CHAIRMAN
BoS /ECE

- Identify the salient features RISC processors based on ARM architecture and different application profiles of ARM core
- Know the features and important specifications of modern microcontrollers
- Explain ARM - M3 architecture and its salient features

TEXT BOOK:

1. K.M.Bhurchandi, A.K Ray, "Advanced Microprocessors and peripherals with ARM and an introduction to microcontrollers and interfacing", 3rd Edition.

REFERENCES:

1. Barry. B. Breg, "The Intel Microprocessors" , PHI,2008.
2. Gene .H.Miller . "Micro Computer Engineering" , Pearson Education , 2003.
3. Intel Inc, "Intel 64 and IA-32 Architectures Developer's Manual", Volume-I, 2016
4. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Newnes, 2010.
5. Scott Mueller, "Upgrading and Repairing PCs", 20th edition, Que.
6. Steve Furber, "ARM System -On -Chip architecture "Addision Wesley , 2000
7. Trevor Martin, "The Designers Guide to the Cortex-M Processor Family", Newnes, 2013

CHAIRMAN
BoS /ECE

PG20MC002	UNIVERSAL HUMAN VALUES 2: UNDERSTANDING HARMONY	L T P C 3 0 0 3

OBJECTIVES:

The students should be made to:

- Understand the need of value education and human aspiration
- Know the difference between self and body
- Recognize the harmony in the family and society
- Understand harmony in nature
- Identify the human values and ethics

UNIT I INTRODUCTION TO VALUE EDUCATION 9

Value Education – need and process, Self-Exploration – process, Basic Human Aspirations - Continuous Happiness and Prosperity, Basic requirement for fulfillment of Human Aspirants, Understanding Happiness and Prosperity – Continuity of Happiness from Physical Facility.

UNIT II HARMONY IN THE HUMAN BEING 9

Human being as a co-existence of the self and the Body - The needs of Self and Body, Body as an Instrument - The Self as the Seer- Doer-Enjoyer, Harmony in the self, Harmony of the Self with the Body –Programme for Self – regulation and health.

UNIT III HARMONY IN THE FAMILY AND SOCIETY 9

Family as the basic unit of human interaction , Understanding Relationship, Trust as the foundational value, Respect as the Right Evaluation, Harmony in the society – Understanding Human Goal, Harmony from Family Order to World Family Order – Universal Human Order - Scope.

UNIT IV HARMONY IN THE NATURE AND EXISTENCE 9

Nature - as Collections of Units, Classification of Units into Four Orders, Interconnectedness, and mutual fulfillment among the four orders of nature, self-regulation in Nature, Understanding Existence as Units in Space, Existence as Co-existence.

UNIT V IMPLICATIONS OF THE ABOVE HOLISTIC UNDERSTANDING OF HARMONY ON PROFESSIONAL ETHICS 9

Natural Acceptance of Human Values - Definitiveness of Ethical Human Conduct, Basis for Humanistic Education, Constitution, Universal Human Order, Competence in Professional Ethics, Holistic Technologies, Production System and Management Models – Typical case, Strategies for Transition towards value based life and profession.

TOTAL: 45 PERIODS

CHAIRMAN
BoS(S&H)

OUTCOMES:

On completion of this course, the students will be able to

- Understand the significance of value education and distinguish between values and skills.
- Distinguish between the Self and the Body, understand the meaning of Harmony in the Self the Co-existence of Self and Body.
- Understand the value of harmonious relationship based on trust, respect and other naturally acceptable feelings.
- Understand the harmony in nature and existence, and work out their mutually fulfilling participation in the nature.
- Distinguish between ethical and unethical practices and understand the human values.

Text Book:

1. R R Gaur, R Sangal, G P Bagaria, 2009, A Foundation Course in Human Values and Professional Ethics, Excel Books, New Delhi, 2nd Revised Edition, 2019.

References:

1. Tripathi A N, "Human Values", New Age Intl. Publishers, New Delhi, 2009.
2. Govindarajan M, Natrajan S and Senthilkumar V S, "Engineering Ethics (Including Human Values)" Eastern Economy, PHI, 12th Edition, 2011.
3. Govindarajan M and Natrajan S, "Professional Ethics and Human Values", PHI, 2011.
4. Banerjee B P, "Foundation of Ethics and Management", Excel Publication, 2005.
5. Bajpai B L, "Indian Ethos and Modern Management", New Royal Book Co, Lucknow, Reprinted 2008.
6. Seebauer and Robert L Berry, "Fundamentals of Ethics for Scientist and Engineers", Oxford University Press, 2000.

CHAIRMAN
BoS(S&H)

20AEEEC301 **PROJECT WORK (PHASE-I)** **L T P C 0 0 12 6**

OBJECTIVES:

The Student should be made to:

- Encourage in identifying problems with social relevance.
- Perform literature survey on recent developments in a selected problem domain.
- Exercise various strategies to find a solution addressing the problem .
- Compare the results with existing methodologies.
- Communicate the work done in written and oral forms.

GUIDELINES TO BE FOLLOWED:

A student should work under a project supervisor, a faculty member and prepare a comprehensive project report after completing the work to the satisfaction of the supervisor. The progress of the project is evaluated based on a minimum of three reviews. The review committee may be constituted by the Head of the Department. A project report is required at the end of the semester. The project work is evaluated based on oral presentation and the project report jointly by external and internal examiners constituted by the Controller of examinations.

The Project Work Phase-I will follow the following Sequence

METHODOLOGY:

I. Problem Identification

1. A statement of system / process specifications proposed to be developed (Block Diagram / Concept tree)
2. List of possible solutions including alternatives and constraints
3. Cost benefit analysis
4. Timeline of activities II.

II. A report highlighting the design finalization [based on functional requirements and standards (if any)]

III.Consolidated report preparation

A report highlighting the design finalization [based on functional requirements and standards (if any)].

A presentation including the following:

1. Implementation Phase (Hardware / Software / both)
2. Testing and Validation of the developed system
3. Learning in the Project

TOTAL: 90 PERIODS

CHAIRMAN
BoS /ECE

OUTCOMES:

On successful completion of this course, the students will be able to,

- Comprehend and identify an industrial or real life problem with solution.
- Execute a proper methodology in problem solving
- Review the literature and design a setup of equipment and complete the analysis
- Write a project report based on the findings
- Demonstrate an ability to present and defend their work to a panel of experts

CHAIRMAN
BoS /ECE

20AEEEC401 **PROJECT WORK (PHASE II)** **L T P C 0 0 24 12**

OBJECTIVES:

The Student should be made to:

- Encourage in identifying problems with social relevance.
- Perform literature survey on recent developments in a selected problem domain.
- Exercise various strategies to find a solution addressing the problem .
- Compare the results with existing methodologies.
- Communicate the work done in written and oral forms.

GUIDELINES TO BE FOLLOWED:

A student should work under a project supervisor, a faculty member and prepare a comprehensive project report after completing the work to the satisfaction of the supervisor. The progress of the project is evaluated based on a minimum of three reviews. The review committee may be constituted by the Head of the Department. A project report is required at the end of the semester. The project work is evaluated based on oral presentation and the project report jointly by external and internal examiners constituted by the Controller of examinations.

The Project Work Phase-II will follow the following Sequence

METHODOLOGY:

1. Student should do it individually.
2. Student should submit / present his/her ideas to the Faculty-in-Charge for approval.
3. Student should submit proposal with system/ technical details and cost implications.
4. Student should periodically demonstrate his/her progress.

EVALUATION:

Evaluation will be based on:

1. The social relevance of the work.
2. The utility of the system developed.
3. The Level of proof of concept.
4. Industry support if obtained.etc

Consolidated report preparation

A report highlighting the design finalization [based on functional requirements and standards (if any)]. A presentation including the following:

1. Implementation Phase (Hardware / Software / both)
2. Testing and Validation of the developed system
3. Learning in the Project

CHAIRMAN
BoS /ECE

TOTAL: 360 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Comprehend and identify an industrial or real life problem with solution.
- Execute a proper methodology in problem solving
- Review the literature and design a setup of equipment and complete the analysis
- Communicate the research findings, in the form of publications in journals, conference proceedings and write a project report based on the findings.
- Demonstrate an ability to present and defend their work to a panel of experts

CHAIRMAN
BoS /ECE

20AEPE101 DIGITAL CONTROL ENGINEERING

L	T	P	C
3	0	0	3

OBJECTIVES:

The Student should be made to:

- Learn the principles of PI, PD, PID controllers.
- Analyze time and frequency response discrete time control system.
- Understand the digital control algorithms.
- Analyze the knowledge of implement in PID control algorithms.
- Develop the schemes for practical implementation of temperature and motor control systems.

UNIT I CONTROLLERS IN FEEDBACK SYSTEMS 9

Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

UNIT II BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS 9

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Describe continuous time and discrete time controllers analytically.
- Define and state basic analog to digital and digital to analog conversion principles.
- Analyze sampled data control system in time and frequency domains.
- Design simple PI, PD, PID continuous and digital controllers.
- Develop schemes for practical implementation of temperature and motor control systems.

REFERENCES:

CHAIRMAN
BoS /ECE

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.
3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.

CHAIRMAN
BoS /ECE

20AEPE102	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand the difference between pipeline and parallel processing concepts
- Study various types of processor architectures and the importance of scalable architectures
- Study memory architectures, memory technology and optimization.
- Design various multiprocessor system
- Implement various multi core architecture system

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES **9**

Fundamentals of Computer Design - Parallel and Scalable Architectures - Multiprocessors - Multi- vector and SIMD architectures - Multithreaded architectures - Stanford Dash multiprocessor - KSR1 - Data-flow architectures Performance Measures.

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP **9**

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling - Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.

UNIT III MEMORY HIERARCHY DESIGN **9**

Memory Hierarchy - Memory Technology and Optimizations - Cache memory - Optimizations of Cache Performance - Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV MULTIPROCESSORS **9**

Symmetric and distributed shared memory architectures - Cache coherence issues - Performance Issues - Synchronization issues - Models of Memory Consistency - Interconnection networks - Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES **9**

Software and hardware multithreading - SMT and CMP architectures - Design issues - Case-studies - Intel Multi-core architecture - SUN CMP architecture - IBM cell architecture - hp architecture.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Assess performance issues and synchronization issues.
- Identify the challenges and issues parallel processing & pipelining
- Learn memory architectures, memory technology and optimization.
- Design various multiprocessor system.
- Know the performance & Compare multicore architectures

CHAIRMAN
BoS /ECE

REFERENCES:

1. David E. Culler, Jaswinder Pal Singh, "Parallel Computing Architecture: A hardware/ software approach", Morgan Kaufmann / Elsevier, 1997
2. Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012
3. Hwang Briggs, "Computer Architecture and parallel processing", McGraw Hill, 1984.
4. John L. Hennessey and David A. Patterson, "Computer Architecture - A quantitative approach", Morgan Kaufmann / Elsevier, 4th edition, 2007
5. John P. Hayes, "Computer Architecture and Organization", McGraw Hill.
6. John P. Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003
7. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001
8. William Stallings, "Computer Organization and Architecture - Designing for Performance", Pearson Education, 7th Edition, 2006

CHAIRMAN
BoS /ECE

20AEPE103	CAD FOR VLSI CIRCUITS	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Study various physical design methods in VLSI.
- Understand the concepts behind the VLSI design rules and routing techniques.
- Understand the concepts of various algorithms used for floor planning and routing techniques
- Learn different simulation and logic synthesis system
- Know the concept of high level synthesis

UNIT I INTRODUCTION TO VLSI DESIGN FLOW **9**

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING **9**

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning.

UNIT III FLOOR PLANNING AND ROUTING **9**

Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS **9**

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS **9**

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- To use the simulation techniques at various levels in VLSI design flow
- Discuss the concepts of floor planning and routing
- understand the concepts of various algorithms used for floor planning and routing
- techniques
- Learn different simulation and logic synthesis system.
- Outline high level synthesis

CHAIRMAN
BoS /ECE

REFERENCES:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
3. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World scientific 1999.
4. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987.

CHAIRMAN
BoS /ECE

20AEPE104	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Study the Electromagnetic Interference concepts
- Learn coupling principles in EMI.
- Identify the Control Techniques.
- Study EMI measurements and standards
- Study instruments and measurements for Electromagnetic Interference

UNIT I BASIC THEORY 9

Introduction to EMI and EMC, Intra-and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

UNIT II COUPLING MECHANISM 9

Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling, Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

UNIT III EMI MITIGATION TECHNIQUES 9

Working principle of Shielding and Murphys Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

UNIT IV STANDARD AND REGULATION 9

Need for Standards, Generic/General Standards for Residential and Industrial environment, Basic Standards, Product Standards, National and International EMI Standardizing Organizations; IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. Electro Magnetic Emission and susceptibility standards and specifications, MIL461E Standards.

UNIT V EMI TEST METHODS AND INSTRUMENTATION 9

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian STD test methods.

TOTAL: 45 PERIODS

CHAIRMAN
BoS /ECE

OUTCOMES:

On successful completion of this course, the students will be able to,

- Understand the electromagnetic interference concepts
- Know the coupling methods.
- Identify the EMI mitigation techniques.
- Analyze the various standard and regulation
- Implement the EMI test methods and Instruments

REFERENCES:

1. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd edition, Artech house, Norwood, 1986.
2. Clayton Paul, "Introduction to Electromagnetic Compatibility", Wiley Interscience, 2006.
3. Daryl Gerke and William Kimmel, "EDN's Designer's Guide to Electromagnetic Compatibility", Elsevier Science & Technology Books, 2002
4. Dr Kenneth L Kaiser, "The Electromagnetic Compatibility Handbook", CRC Press 2005.
5. Norman Violette, "Electromagnetic Compatibility", Published by Springer, 2013
6. Donald R. J, "Electromagnetic Interference and Compatibility: Electrical noise and EMI specifications Volume 1 of A Handbook Series on Electromagnetic Interference and Compatibility", White Publisher-Don white consultants Original from the University of Michigan Digitized 6 Dec 2007
7. Henry W. Ott, "Electromagnetic Compatibility Engineering", John Wiley & Sons Inc, Newyork, 2009
8. V Prasad Kodali, "Engineering Electromagnetic Compatibility", IEEE Press, Newyork, 2001.
9. W Scott Bennett, "Control and Measurement of Unintentional Electromagnetic Radiation", John Wiley & Sons Inc., (Wiley Interscience Series) 1997.

CHAIRMAN
BoS /ECE

20AEPE201	VLSI DESIGN TECHNIQUES	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Describe transistor level design and CMOS inverter
- Understand the combinational logic and issues related to power consumption.
- Know the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.
- Know the design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- Understand the interconnect and clocking strategies in digital systems.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmores constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 9

Interconnect Parameters - Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block
- Analyze tradeoffs of the various circuit choices for each of the building block.
- Have idea about performance of arithmetic blocks and memory architectures.
- Analyze interconnect and clocking strategies for digital systems.

CHAIRMAN
BoS /ECE

REFERENCES:

- Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, 3rd Edition", Wiley IEEE Press 2010.
- Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Prentice Hall of India 2nd Edition, Feb 2003,
- M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
- N.Weste, K. Eshraghian, "Principles of CMOS VLSI Design". Addision Wesley, 2nd Edition, 1993

CHAIRMAN
BoS /ECE

20AEPE202 **NANO ELECTRONICS** **L T P C**
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand how transistor as nano device and different types of nano devices.
- Understand various forms of nano Devices
- Understand the Nano Sensors.
- Know the choices of materials in gas sensors.
- Know about the principles of biosensors

UNIT I SEMICONDUCTOR NANO DEVICES **9**

Single-Electron Devices; Nano scale MOSFET - Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.

UNIT II ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS **9**

Preparation - Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs- LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT III THERMAL SENSORS **9**

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV GAS SENSOR MATERIALS **9**

Criteria for the choice of materials - Experimental aspects - materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V BIOSENSORS **9**

Principles - DNA based biosensors - Protein based biosensors - materials for biosensor applications - fabrication of biosensors - future potential.

TOTAL: 45 PERIODS

Outcome:

At the end of the course, the student should be able to:

- Simulate and design the nano device.
- Usage of photonic and electronic materials in nano devices.
- Simulate and design the nano sensors.
- Gain knowledge in sensors based on semiconductor devices.
- Know the usage of biosensors & its applications.

CHAIRMAN
BoS /ECE

REFERENCES:

1. K.E. Drexler, "Nano systems", Wiley,1992.
2. M.C. Petty, "Introduction to Molecular Electronics", 1995.
3. W. Ranier, "Nano Electronics and Information Technology", Wiley, 2003.

CHAIRMAN
BoS /ECE

20AEPE203	WIRELESS ADHOC AND SENSOR NETWORKS	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand the basics of Ad-hoc & Sensor Networks.
- Learn various fundamental and emerging protocols of all layers.
- Study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
- Understand the nature and applications of Ad-hoc and sensor networks.
- Understand various security practices and protocols of Ad-hoc and Sensor Networks.

UNIT I MAC & TCP IN AD HOC NETWORKS **9**

Fundamentals of WLANs - IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks - MAC Protocols for Ad-Hoc Wireless Networks - Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs - Solutions for TCP over Ad-Hoc Networks.

UNIT II ROUTING IN AD HOC NETWORKS **9**

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues - Location services - DREAM - Quorums based location service - Grid - Forwarding strategies - Greedy packet forwarding - Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT III MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS **9**

Introduction - Architecture - Single node architecture - Sensor network design considerations - Energy Efficient Design principles for WSNs - Protocols for WSN - Physical Layer : Transceiver Design considerations - MAC Layer Protocols - IEEE 802.15.4 Zigbee - Link Layer and Error Control issues - Routing Protocols - Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking - Transport Protocols & QOS - Congestion Control issues - Application Layer support.

UNIT IV SENSOR MANAGEMENT **9**

Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization Localization and positioning - Operating systems and Sensor Network programming - Sensor Network Simulators.

UNIT V SECURITY IN AD HOC AND SENSOR NETWORKS **9**

Security in Ad-Hoc and Sensor networks - Key Distribution and Management - Software based Anti-tampertechniques - water marking techniques - Defense against routing attacks - Secure Adhoc routing protocols - Broadcast authentication WSN protocols - TESLA - Biba - Sensor Network Security Protocols - SPINS.

TOTAL: 45 PERIODS

CHAIRMAN
BoS /ECE

OUTCOMES:

On successful completion of this course, the students will be able to,

- Identify different issues in wireless ad hoc and sensor networks.
- To analyze protocols developed for ad hoc and sensor networks.
- Knowledge about quality of service in ad hoc and sensor networks.
- Establish a Sensor network environment for different type of applications.
- To identify and address the security threats in ad hoc and sensor networks.

REFERENCES:

1. Adrian Perrig, J. D. Tygar, "Secure Broadcast Communication: In Wired and Wireless Networks", Springer, 2006.
2. Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc and Sensor Networks: Theory and Applications", 2nd Edition, World Scientific Publishing, 2011
3. C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks - Architectures and Protocols", Pearson Education, 2004.
4. C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2002.
5. Erdal yrc , Chunming Rong, "Security in Wireless Ad Hoc and Sensor Networks", John Wiley and Sons, 2009.
6. Holger Karl, Andreas willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley & Sons, Inc .2005.
7. Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, "Ad Hoc Mobile Wireless Networks", Auerbach Publications, 2008.
8. Waltenegus Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks Theory and Practice", John Wiley and Sons, 2010.

CHAIRMAN
BoS /ECE

20AEPE204	HIGH PERFORMANCE NETWORKS	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Know the performance of different networks.
- Develop a comprehensive understanding of multimedia networking.
- Study the types of VPN and tunneling protocols for security.
- Understand the different types of traffic modeling.
- Learn about network security in many layers and network management.

UNIT I INTRODUCTION **9**

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET - DWDM - DSL - ISDN - BISDN, ATM.

UNIT II MULTIMEDIA NETWORKING APPLICATIONS **9**

Streaming stored Audio and Video - Best effort service - protocols for real time interactive applications - Beyond best effort - scheduling and policing mechanism - integrated services - RSVP- differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS **9**

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS-operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks- P2P connections.

UNIT IV TRAFFIC MODELLING **9**

Little's theorem, Need for modeling, Poisson modeling and its failure, Non- Poisson models, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT **9**

Principles of cryptography - Authentication - integrity - key distribution and certification - Access control and: fire walls - attacks and counter measures - security in many layers. Infrastructure for network management - The internet standard management framework - SMI, MIB, SNMP, Security and administration - ASN.1.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Have knowledge in performance of different networks.
- Understand the integrated and differentiated services.
- Discuss advanced networks concepts
- Outline traffic modeling
- Evaluate network security and management.

CHAIRMAN
BoS /ECE

REFERENCES:

1. Aunurag Kumar, D. M Anjunath, Joy Kuri, "Communication Networking", Morgan Kaufmann Publishers, 1st edition 2004.
2. Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet", 5th edition, Pearson education 2006
3. Hersent Gurle & Petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003
4. J.F. Kurose & K.W. Ross, "Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003
5. Larry l. Peterson & Bruce S.David, "Computer Networks: A System Approach"- 1996
6. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH 7th reprint 2002.
7. Nader F.Mir , "Computer and Communication Networks, 1st edition 2010
8. Walrand .J. Varatya, "High performance communication network", Morgan Kauffman - Harcourt Asia Pvt. Ltd. 2nd Edition, 2000

CHAIRMAN
BoS /ECE

20AEPE205	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand the fundamentals of Digital Signal Processor.
- Know the special functions & programming skill for realtime applications.
- Understand the tools used for linear programming.
- Know the Third generation DSP Architecture and programming skills.
- Advanced DSP architectures and some applications.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSP'S **9**

Multiplier and Multiplier accumulator - Modified Bus Structures and Memory access in PDSPs - Multiple access memory - Multi-port memory - VLIW architecture- Pipelining - Special Addressing modes in P-DSPs - On chip Peripherals.

UNIT II SPECIAL FUNCTIONS **9**

Architecture - Assembly language syntax - Addressing modes - Assembly language Instructions - Pipeline structure, Operation - Block Diagram of DSP starter kit - Application Programs for processing real time signals.

UNIT III LINEAR PROGRAMMING **9**

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction - DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools - Application Programs for processing real time signals.

UNIT IV ALGEBRAIC EQUATIONS **9**

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions - Application programs -Filter design, FFT calculation.

UNIT V ORDINARY DIFFERENTIAL EQUATIONS **9**

Architecture of TMS320C54X: Pipe line operation, Code Composer studio - Architecture of TMS320C6X - Architecture of Motorola DSP563XX - Comparison of the features of DSP family processors.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Have knowledge in programmable DSP's
- Become Digital Signal Processor specialized engineer
- Familiarize with tools used in DSP based System
- Analyze the performance of advanced DSP"s.
- Understand the architecture of different processors.

CHAIRMAN
BoS /ECE

REFERENCES:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing - Implementations using DSP Microprocessors with Examples from TMS320C54xx", cengage Learning India Private Limited, Delhi 2012
2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors - Architecture, Programming and Applications", Tata McGraw - Hill Publishing Company Limited. New Delhi, 2003.
3. Rulph Chassaing, "Digital Signal Processing and Applications with the C6713 and C6416 DSK", A John Wiley & Sons, Inc., Publication, 2005.

CHAIRMAN
BoS /ECE

20AEPE206 **RF SYSTEM DESIGN** L T P C
3 0 0 3

OBJECTIVES:

The Student should be made to:

- Understand the CMOS physics,tranceivrs and its architectures..
- Know the importance of impedance matching circuits.
- Understand the operation of power amplifiers and effects of feedback systems.
- Understand the performance of different oscillators used in RF systems.
- Understand the operation of PLL and frequency synthesizer.

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model - Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

UNIT IV MIXERS AND OSCILLATORS 9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Carry out transistor level design of the entire RFE.
- Have knowledge in designing of impedance matching circuits.
- Analyze the performance of feedback systems and amplifiers.

CHAIRMAN
BoS /ECE

- Design a mixer and oscillators for any applications.
- Know the importance of PLL and frequency synthesizer.

REFERENCES :

- B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001
- B.Razavi, "RF Microelectronics", Pearson Education, 1997.
- Jan Crols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997.
- T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004.

ONLINE RESOURCES:

- Recorded lectures and notes available at http://www.ee.iitm.ac.in/ ani/ee6240/

CHAIRMAN
BoS /ECE

20AEPE207	SPEECH AND AUDIO SIGNAL PROCESSING	L T P C 3 0 0 3

OBJECTIVES:

The Student should be made to:

- Study basic concepts of processing speech and audio signals
- Study and analyse various M-band filter-banks for audio coding
- Understand audio coding based on transform coders.
- Study time and frequency domain speech processing methods.
- Study about various methods of predictive analysis speech processing.

UNIT I MECHANICS OF SPEECH AND AUDIO 9

Introduction - Review of Signal Processing Theory-Speech production mechanism - Nature of Speech signal - Discrete time modelling of Speech production - Classification of Speech sounds - Phones - Phonemes - Phonetic and Phonemic alphabets - Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non- simultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS 9

Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks - Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies.

UNIT III AUDIO CODING AND TRANSFORM CODERS 9

Lossless Audio Coding - Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder - Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding - Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization - MDCT with Vector Quantization.

UNIT IV TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING 9

Time domain parameters of speech signal - methods for extracting the parameters :energy, average magnitude - zero crossing rate - silence discrimination using zcr and energy short time fourier analysis - formant extraction - pitch extraction using time and frequency domain methods homomorphic speech analysis: cepstral analysis of speech - formant and pitch estimation - homomorphic vocoders.

CHAIRMAN
BoS /ECE

UNIT V PREDICTIVE ANALYSIS OF SPEECH **9**

Formulation of Linear Prediction problem in Time Domain - Basic Principle - Auto correlation method - Covariance method - Solution of LPC equations - Cholesky method - Durbin's Recursive algorithm - lattice formation and solutions - Comparison of different methods - Application of LPC parameters - Pitch detection using LPC parameters - Formant analysis - VELP - CELP.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Evaluate audio coding and transform coders.
- Know about different filter banks and its features.
- Analyze the different types of audio coding and transform coders.
- Discuss time and frequency domain methods for speech processing.
- Explain predictive analysis of speech

REFERENCES :

1. B.Gold and N.Morgan, "Speech and Audio Signal Processing", Wiley and Sons, 2000.
2. L.R.Rabiner and R.W.Schaffer, "Digital Processing of Speech Signals", Prentice Hall, 1978.
3. Mark Kahrs, Karlheinz Brandenburg, Kluwer Applications of Digital Signal Processing to Audio And Acoustics, Academic Publishers,
4. Udo Zlzer, "Digital Audio Signal Processing", Second Edition A John Wiley & sons Ltd

CHAIRMAN
BoS /ECE

20AEPE208 SOLID STATE DEVICE MODELLING AND SIMULATION

L	T	P	C
3	0	0	3

OBJECTIVES:

The Student should be made to:

- Understand the MOSFET device modeling.
- Understand the concept of device modeling.
- Learn multistep method
- Study device simulations
- Know the different types devices simulation and signal analysis.

UNIT I MOSFET DEVICE PHYSICS MOSFET **9**

Capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II DEVICE MODELLING **9**

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III MULTISTEP METHODS **9**

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS **9**

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES **9**

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, the students will be able to,

- Have knowledge in MOSFET device modeeling
- Analyze circuits using parasitic BJT parameters and newton Raphson method.
- Model the MOS transistor using schrodinger equation and Multistep methods.
- Apply and determine the drift diffusion equation and stiff system equation.
- Explain the importance of MOS Capacitor and Small signal modeling

CHAIRMAN
BoS /ECE

REFERENCES :

1. Arora, N., "MOSFET Modeling for VLSI Simulation", Cadence Design Systems, 2007
2. Chua, L.O. and Lin, P.M., "Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques", Prentice-Hall., 1975
3. Fjeldly, T., Yetterdal, T. and Shur, M., "Introduction to Device Modeling and Circuit Simulation", Wiley-Interscience., 1997
4. Grasser, T., "Advanced Device Modeling and Simulation", World Scientific Publishing Company., 2003
5. Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag.,1984
6. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.

CHAIRMAN
BoS /ECE

20AEPE301	INTERNET OF THINGS	L T P C 3 0 0 3

OBJECTIVES:

The students should be made to

- Understand the fundamentals of Internet of Things
- Learn about the basics of IOT protocols
- Build a small low cost embedded system using Raspberry Pi.
- Apply the concept of Internet of Things in the real world scenario
- Implement the real world applications

UNIT I INTRODUCTION TO IOT **9**

Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology.

UNIT II IOT ARCHITECTURE **9**

M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture.

UNIT III IOT PROTOCOLS **9**

Protocol Standardization for IoT - Efforts - M2M and WSN Protocols - SCADA and RFID Protocols - Unified Data Standards - Protocols - IEEE 802.15.4 - BACNet Protocol - Modbus-Zigbee Architecture - Network layer - 6LowPAN - CoAP - Security.

UNIT IV BUILDING IOT WITH RASPBERRY PI & ARDUINO **9**

Building IOT with RASPERRY PI- IoT Systems - Logical Design using Python - IoT Physical Devices & Endpoints IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms - Arduino.

UNIT V CASE STUDIES AND REAL-WORLD APPLICATIONS **9**

Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT - Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT -Amazon Web Services for IoT.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Analyze various protocols for IoT
- Develop web services to access/control IoT devices.
- Design a portable IoT using Rasperry Pi

CHAIRMAN
BoS /ECE

- Deploy an IoT application and connect to the cloud.
- Analyze applications of IoT in real time scenario

TEXT BOOK:

1. Internet of Things: Technologies and Applications for a New Age of Intelligence Vlasios Tsiatsis, Senior Researcher at Ericsson Research, Sweden 2nd edition

REFERENCES:

1. Arshdeep Bahga, Vijay Madisetti, "Internet of Things - A hands-on approach", Universities Press, 2015
2. Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), "Architecting the Internet of Things", Springer, 2011.
3. Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.
4. Jan Holler, Vlasios Tsiatsis , Catherine Mulligan, Stamatis , Karnouskos, Stefan Avesand. David Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.
5. Olivier Hersent, David Boswarthick, Omar Elloumi , "The Internet of Things - Key applications and Protocols", Wiley, 2012

CHAIRMAN
BoS /ECE

20AEPE302 SYSTEM ON CHIP DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The students should be made to

- Understand the basics of system on chip design
- Learn about the basics system level modelling
- Analyze the virtual platform models co-simulation and FPGA .
- Apply the concept of TLM, RTL architecture, Pipelining and scheduling
- Implement the SOC verification and testing

UNIT I INTRODUCTION 9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design.

UNIT II SYSTEM LEVEL MODELLING 9

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples.

UNIT III HARDWARE SOFTWARE CO-DESIGN 9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV SYNTHESIS 9

System synthesis: Transaction Level Modelling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimization, resource sharing and pipelining and scheduling.

UNIT V SOC VERIFICATION AND TESTING 9

SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Analyse algorithms and architecture of hardware software inorder to optimise the system based on requirements and implementation constraints
- Model and specify systems at high level of abstraction
- Appreciate the co-design approach and virtual platform models

CHAIRMAN
BoS /ECE

- Understand hardware, software and interface synthesis
- Analyze the application of system on chip design

TEXT BOOK:

1. M. Wolf, "Computer as Components: Principles of Embedded Computing System Design", 3rd or 4th edition Morgan Kaufmann-Elsevier Publishers 2012, 2016

REFERENCES:

1. D. Black, J. Donovan, "SystemC: From the Ground Up", Springer, 2004.
2. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, "Embedded System Design: Modeling, Synthesis, Verification", Springer, 2009
3. Erik Larson, "Introduction to advanced system-on-chip test design and optimization", Springer 2005
4. Grotker, T., Liao, S., Martin, G. & Swan, S., "System design with System C", Springer, 2002.
5. Ghenassia, F. "Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems", Springer, 2010.
6. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, "Low power NoC for high performance SoC desing",CRC press, 2008.
7. M. L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits", Springer, 2005
8. M. Abramovici, M. Breuer, and A. Friedman, "Digital System Testing and Testable Design", IEEE Press, 1994
9. P. Marwedel, "Embedded System Design", Springer, 2003.
10. G. De Micheli, "Synthesis and Optimization of Digital Circuits"
11. Prakash Rashinkar, Peter Paterson and Leena Singh, "System-on-a chip verification: Methodology and techniques", kluwer Academic Publishers 2002

CHAIRMAN
BoS /ECE

20AEPE303 **ROBOTICS** L T P C
3 0 0 3

OBJECTIVES:

The students should be made to:

- Understand robot locomotion and mobile robot kinematics
- Learn about perception in robotics with place recognition range data
- Analyze the mobile robot localization with UKF localization
- Understand simultaneous localization and mapping (SLAM)
- Know the concept of robot planning and navigation

UNIT I LOCOMOTION AND KINEMATICS 9

Introduction to Robotics - key issues in robot locomotion - legged robots - wheeled mobile robots - aerial mobile robots - introduction to kinematics - kinematics models and constraints - robot maneuverability.

UNIT II ROBOT PERCEPTION 9

Sensors for mobile robots - vision for robotics - cameras - image formation - structure from stereo - structure from motion - optical flow - color tracking - place recognition - range data.

UNIT III MOBILE ROBOT LOCALIZATION 9

Introduction to localization - challenges in localization - localization and navigation - belief representation - map representation - probabilistic map-based localization - Markov localization - EKF localization - UKF localization - Grid localization - Monte Carlo localization - localization in dynamic environments.

UNIT IV MOBILE ROBOT MAPPING 9

Autonomous map building - occupancy grip mapping - MAP occupancy mapping - SLAM - extended Kalman Filter SLAM - graph-based SLAM - particle filter SLAM - sparse extended information filter – fast SLAM algorithm.

UNIT V PLANNING AND NAVIGATION 9

Introduction to planning and navigation - planning and reacting - path planning - obstacle avoidance techniques - navigation architectures - basic exploration algorithms.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Apply kinematics models and constraints
- Implement vision algorithms for robotics
- Analyze the robot localization techniques
- Implement robot mapping techniques and implement SLAM algorithms
- Explain planning and navigation in robotics

CHAIRMAN
BoS /ECE

TEXT BOOK:

1. Anis Koubaa Hachemi Bennaceur,Imen Chaari, "Robot Path Planning and Cooperation: Foundations, Algorithms and Experimentations", Springer International Publishing.

REFERENCES:

1. Gregory DudekandMichael Jenkin, "Computational Principles of Mobile Robotics", Second Edition, Cambridge University Press, 2010.
2. Howie Choset et al., "Principles of Robot Motion: Theory, Algorithms, and Implementations", A Bradford Book, 2005.
3. Maja J. Mataric, "The Robotics Primer", MIT Press, 2007.
4. Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, "Introduction to autonomous mobile robots", Second Edition, MIT Press, 2011.
5. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, "Probabilistic Robotics", MIT Press, 2005.

CHAIRMAN
BoS /ECE

20AEPE304 **OPTICAL NETWORKS** L T P C
3 0 0 3

OBJECTIVES:

The students should be made to

- Learn the basic Optical system components
- Understand Optical amplifiers, wavelength converters.
- Gain knowledge in SONET and SDH
- Study different types of network topologies.
- Understand different protection schemes

UNIT I INTRODUCTION TO OPTICAL NETWORKS 9

Introduction to Optical Networks: Telecommunications Networks Architecture, Services, circuit switching and packet switching, Optical Networks: Multiplexing Techniques, Second generation Optical Networks, Optical Packet Switching, Transmission Basics: Wavelength, frequencies, and channel spacing, Wavelength standards, Optical power and loss, Network Evolution, Nonlinear Effects: Self-phase Modulation, Cross-phase Modulation, Four Wave mixing, Solitons. Components: Couplers, Isolators and Circulators, Multiplexers and Filters, Optical Amplifiers, Transmitters, Detectors, Switches, Wavelength Converters.

UNIT II TRANSMISSION SYSTEM ENGINEERING 9

Transmission System Engineering: System Model, Power Penalty, Transmitter, Receiver, Optical Amplifiers, Crosstalk, Dispersion, Wavelength Stabilization, Overall Design Considerations. Optical Internets: Migration to IP optical networking, IP and Optical backbone, IP Routing table, MPLS and optical cross connect table, Protocol stack Alternatives, Internetworking SS7 and Legacy Transport, Internet transport network protocol stack.

UNIT III SONET AND SDH 9

SONET, SDH and Optical Transport Networks (OTNs): SONET and SDH: SONET multiplexing hierarchy, Frame structure, Functional Component, problem detection, concatenation. Architecture of Optical Transport Networks (OTNs): Digital wrapper, in-band and out-of band control signalling, Importance of Multiplexing and multiplexing hierarchies, SONET multiplexing hierarchies, SDH multiplexing hierarchies, New Optical Transport, OTN layered Model, Generic Framing Procedure (GFP)

UNIT IV NETWORK TOPOLOGIES 9

WDM, Network topologies, MPLS and Optical Networks: WDM: WDM operation, Dense Wavelength Division Multiplexing (DWDM), Erbium-doped Fiber (EDF), WDM amplifiers, Add-Drop Multiplexers, Wavelength Continuity Property, Higher dispersion for DWDM, Tunable DWDM Lasers.

UNIT V PROTECTION SCHEMES 9

Network topologies and protection schemes: Robust networks, Line and path protection switching, Types of topology, Point to point topology, bi-directional line-switched ring (BLSR), meshed topology, Passive optical networks, Metro optical networks 28 MPLS and Optical Networks: IS label switching, Forwarding equivalence class (FEC), Types of MPLS nodes, Label distribution and binding, label swapping and traffic forwarding, MPLS support of Virtual Private Networks (VPN), MPLS traffic engineering, Multi protocol Lambda switching (MPIS).

CHAIRMAN
BoS /ECE

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Design and Analyze Network Components
- Learn various Optical Network Architecture
- Ability to understand the frame structure and functional components of SONET/SDH
- Knowledge on network topologies.
- Assess and Evaluate optical networks

REFERENCES:

1. Rajiv Ramaswami and Kumar Sivarajan, "Optical Networks – Practical Perspective", 3rd Edition, Morgan - Kaufmann Publishers.
2. Optical Networks, Third Generation Transport Systems, Uyless Black, Pearson 18

CHAIRMAN
BoS /ECE

20AEPE305 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN

L	T	P	C
3	0	0	3

OBJECTIVES:

The students should be made to:

- Identify sources affecting the speed of digital circuits.
- Introduce methods to improve the signal transmission characteristics
- Analyze the non ideal effects for BGA fields
- Learn the concept of power consideration and system design
- Understand the clock distribution and clock oscillators techniques

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations - L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk,minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths - gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses - Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling , Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

CHAIRMAN
BoS /ECE

- Analyze the non ideal effects for BGA fields
- Understand the concept of power consideration and system design
- Design the techniques for clock distribution and clock oscillators

TEXT BOOKS:

1. Stephen h. Hall howard, Heck a john "Advanced signal integrity for high-speed digital design" wiley & sons, inc., IEEE

REFERENCES:

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003
2. Eric Bogatin, "Signal Integrity - Simplified, Prentice Hall PTR, 2003.
3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

ONLINE RESOURCES:

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

CHAIRMAN
BoS /ECE

20AEPE306 **MEMS AND NEMS** L T P C
3 0 0 3

OBJECTIVES:

The students should be made to

- Introduce the concepts of micro electromechanical devices.
- Know the fabrication process of Microsystems.
- Know the design concepts of micro sensors and micro actuators.
- Familiarize concepts of quantum mechanics and nano systems.
- Learn the method of Nano systems and quantum mechanics

UNIT I OVERVIEW 9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS - Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Micro system fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V NANO SYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Discuss different application of MEMS and NEMS Nano scale systems
- Explain MEMS fabrication , Surface Micromachining and Selection of packaging materials

CHAIRMAN
BoS /ECE

- Discuss about micro sensors with piezo resistive pressure sensor
- Understand the micro actuators with Micromechanical Motors
- Outline nano systems and Quantum mechanics

TEXT BOOK:

1. Cornelius T. Leondes, "Mems/Nems- Handbook Techniques and Applications", Springer, 2012

REFERENCES:

1. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006.
2. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997
3. Stephen D. Senturia, "Micro system Design", Kluwer Academic Publishers,2001
4. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.
5. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture" ,Tata McGraw Hill, 2002

CHAIRMAN
BoS /ECE

20AEPE307 **SECURE COMPUTING SYSTEMS** L T P C
3 0 0 3

OBJECTIVES:

The students should be made to

- Learn computer hardware, system software and data concepts from a security perspective
- Know the concept of hardware security with unclonable functions
- Design the assembly and operating systems security
- Learn the advanced computer architecture with virtualization
- Implement the different network and web security

UNIT I COMPUTER SECURITY AND MANAGEMENT 9

Overview of Computer Security, Threats, Malware, Vulnerabilities, Authentication, Access Control, Security Management Models, Security Management Practices, Protection Mechanisms, Legal aspects of security, Ethical Hacking.

UNIT II HARDWARE SECURITY 9

Need for Hardware Security, Computer Memory and storage, Bus and Interconnection, I/O and Network Interface, CPU; Side channel Analysis: Power Analysis Attack, Timing Attack, Fault attack. Countermeasures of Side Channel Attack, Secure Hardware Intellectual Properties, Physically Unclonable Functions(PUFs), Secure PUF.

UNIT III ASSEMBLY AND OPERATING SYSTEMS SECURITY 9

Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions.

UNIT IV ADVANCED COMPUTER ARCHITECTURE 9

Security aspects : Multiprocessors, parallel processing, Ubiquitous computing, Grid, Distributed and cloud computing, Internet computing, Virtualization.

UNIT V NETWORK AND WEB SECURITY 9

TCP/IP Protocol, Network switches, Routers, Gateways, Wireless Networks and Network Address Translation (NAT); Network Security Issues in TCP/IP, Threat Models, Denial of Service Attacks, Firewalls, Intrusion Detection, Browser Attacks, Web Attacks Targeting Users, Email Attacks, Secure Shell (SSH), HTTPS.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Aware of Security aspects and other management models
- Able to appreciate security in hardware, OS and it future need
- Learn about assembly and operating systems security
- Learn security issues in various types of computing networks
- Implement the different network and web security

CHAIRMAN
BoS /ECE

TEXT BOOK:

1. Gregory B. White,Eric A. Fisch,,Udo W. Pooch, "Computer System and Network Security" 1st edition,1996.

REFERENCES:

1. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security in Computing", 4th Edition, Pearson Education, 2007
2. Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, "Hardware Security - Design Threats and Safeguards", CRC Press, 2015
3. Michael Whitman, Herbert J. Mattord, "Management of Information Security", 3rd Edition, Course Technology, 2010
4. Shuangbao Wang, Robert S. Ledley, "Computer Architecture and Security", Wiley, 2013
5. William Stallings, "Network Security Essentials, Applications and Standards", Dorling Kindersley I P Ltd, Delhi, 2008.

CHAIRMAN
BoS /ECE

20AEPE308 **PATTERN RECOGNITION** L T P C
3 0 0 3

OBJECTIVES:

The students should be made to

- Learn about supervised and unsupervised pattern classifiers.
- Familiarize about different feature extraction techniques.
- Explore the role of Hidden Marko model and SVM in pattern recognition.
- Understand the application of Fuzzy logic and genetic algorithms for pattern classifier
- Implement the recent advance technology

UNIT I PATTERN CLASSIFIER 9

Overview of Pattern recognition - Discriminant functions - Supervised learning - Parametric estimation - Maximum Likelihood Estimation - Bayesian parameter Estimation - Problems with Bayes approach- Pattern classification by distance functions - Minimum distance pattern classifier.

UNIT II CLUSTERING 9

Clustering for unsupervised learning and classification-Clustering concept - C Means algorithm - Hierarchical clustering - Graph theoretic approach to pattern Clustering - Validity of Clusters.

UNIT III FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION 9

Principle component analysis, Independent component analysis, Linear discriminant analysis, Feature selection through functional approximation - Elements of formal grammars, Syntactic description - Stochastic grammars - Structural Representation.

UNIT IV HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE 9

State Machines - Hidden Markov Models - Training - Classification - Support vector Machine - Feature Selection.

UNIT V RECENT ADVANCES 9

Fuzzy logic - Fuzzy Pattern Classifiers - Pattern Classification using Genetic Algorithms - Case Study Using Fuzzy Pattern Classifiers and Perception.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Differentiate between supervised and unsupervised classifiers
- Classify the data and identify the patterns.
- Extract feature set and select the features from given data set.
- Apply fuzzy logic and genetic algorithms for classification problems
- Implement the different real time advance technology

CHAIRMAN
BoS /ECE

TEXT BOOK:

1. Dougherty, Geoff, "Pattern Recognition and Classification, an Introduction", Springer.

REFERENCES:

1. Andrew Webb, "Stastical Pattern Recognition", Arnold publishers, London, 1999
2. C.M.Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.
3. M. Narasimha Murthy and V. Susheela Devi, "Pattern Recognition", Springer 2011.
4. Menahem Friedman, Abraham Kandel, "Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches", World Scientific publishing Co. Ltd, 2000.
5. Robert J.Schalkoff, "Pattern Recognition Statistical, Structural and Neural Approaches", John Wiley & Sons Inc., New York, 1992.
6. R.O.Duda, P.E.Hart and D.G.Stork, "Pattern Classification", John Wiley, 2001
7. S.Theodoridis and K.Koutroumbas, "Pattern Recognition", 4th Edition, Academic Press. 2009.

CHAIRMAN
BoS /ECE