



(<http://ipindia.nic.in/index.htm>)



(<http://ipindia.nic>)

Patent Search

Invention Title	LABELING TECHNIQUES IN FAULT-TOLERANT COMPUTING SYSTEMS: THEORETICAL FOUNDATIONS AND APPLICATIONS
Publication Number	47/2023
Publication Date	24/11/2023
Publication Type	INA
Application Number	202341067237
Application Filing Date	06/10/2023
Priority Number	
Priority Country	
Priority Date	
Field Of Invention	COMPUTER SCIENCE
Classification (IPC)	G06F0016901000, H01L0025000000, H04L0045500000, H01L0025100000, G01R0033563000

Inventor

Name	Address	Country
Dr. P. Shyamala Anto Mary	Assistant Professor, College Name With Address: Department Of Mathematics, Srm Trp Engineering College, Irungalur, Tiruchirappalli, Pin: 621105, Tamilnadu, India.	India
Dr. K.Deiwakumari	Assistant Professor, Sona College Of Technology, Junction Main Road, Suramangalam, Salem, Pin: 636 005, Tamil Nadu, India.	India
Dr. G. Kavitha	Associate Professor, Selvamm Arts And Science College, Namakkal, Pin:637003, Tamilnadu, India.	India
Dr. P. Thangavel	Assistant Professor, Srm Trichy Arts And Science College, Tiruchirappalli, Pin: 621105, Tamilnadu, India.	India
Dr. K. Balasubramanian	Professor/Mathematics, Kongunadu College Of Engineering And Technology (Autonomous), Thottiam, Tiruchirappalli, Pin:621215, Tamilnadu, India.	India
Pitchaimani.T	Assistant Professor, K.Ramakrishnan College Of Technology, Samayapuram, Tiruchirappalli, Pin:621112 State: Tamilnadu, India	India
Mr.T.Udhayakumar	Assistant Professor, Department Of Cse, Rathinam Technical Campus, Coimbatore, Pin:641021, Tamilnadu, India.	India
Ms.Kanakaprabha. S	Assistant Professor, Department Of Computer Science And Engineering, Rathinam Technical Campus Coimbatore, Pin: 641021, Tamilnadu, India.	India
Dr.G.Ganesh Kumar	Associate Professor, Rathinam Technical Campus, Pollachi Main Road, Eachanari, Coimbatore. Pin:641021, Tamilnadu, India.	India
Dr. Harikumar Pallathadka	Director And Professor, Manipur International, University, Ghari, Imphal, Imphal West, Imphal, Pin: 795140, Manipur, India.	India

Applicant

Name	Address	Country
Dr. P. Shyamala Anto Mary	Assistant Professor, College Name With Address: Department Of Mathematics, Srm Trp Engineering College, Irungalur, Tiruchirappalli, Pin: 621105, Tamilnadu, India.	India
Dr. K.Deiwakumari	Assistant Professor, Sona College Of Technology, Junction Main Road, Suramangalam, Salem, Pin: 636 005, Tamil Nadu, India.	India
Dr. G. Kavitha	Associate Professor, Selvamm Arts And Science College, Namakkal, Pin:637003, Tamilnadu, India.	India
Dr. P. Thangavel	Assistant Professor, Srm Trichy Arts And Science College, Tiruchirappalli, Pin: 621105, Tamilnadu, India.	India
Dr. K. Balasubramanian	Professor/Mathematics, Kongunadu College Of Engineering And Technology (Autonomous), Thottiam, Tiruchirappalli, Pin:621215, Tamilnadu, India.	India
Pitchaimani.T	Assistant Professor, K.Ramakrishnan College Of Technology, Samayapuram, Tiruchirappalli, Pin:621112 State: Tamilnadu, India	India
Mr.T.Udhayakumar	Assistant Professor, Department Of Cse, Rathinam Technical Campus, Coimbatore, Pin:641021, Tamilnadu, India.	India
Ms.Kanakaprabha. S	Assistant Professor, Department Of Computer Science And Engineering, Rathinam Technical Campus, Coimbatore, Pin: 641021, Tamilnadu, India.	India
Dr.G.Ganesh Kumar	Associate Professor, Rathinam Technical Campus, Pollachi Main Road, Eachanari, Coimbatore. Pin:641021, Tamilnadu, India.	India
Dr. Harikumar Pallathadka	Director And Professor, Manipur International, University, Ghari, Imphal, Imphal West, Imphal, Pin: 795140, Manipur, India.	India

Abstract:

Labeling Techniques in Fault-Tolerant Computing Systems: Theoretical Foundations and Applications Abstract One of the most essential concepts that is vital for the c of integrated circuits for electrical devices is graph theory. These parts, known as chips, are made up of intricate, multilayer microcircuits that can be visualised as coll points connected by lines or arcs. Utilizing graph theory, engineers create integrated chips with the highest component density and the shortest overall interconnecti length. This is crucial for improving processing speed and electricity efficiency. This study provides an overview of prime graph labeling with a focus on creating fault-t systems with facility graphs. Key words: Grotzsch graph, graph labeling, prime labeling, duplication, switching and path union.

Complete Specification**Description: I. INTRODUCTION**

Many researchers have been drawn to the idea of prime labeling because prime number theory is essential and because the sequence of prime numbers contains : huge gaps and prime numbers that are dispersed throughout. Many results on prime labelling have been looked into by Vaidya and Prajapati. Prime labelling has b considered by the same authors in relation to duplicate graph elements. Inspired by the ideas of prime labelling and cordial labelling, Sundaram developed a brand idea called prime cordial labelling that combines both els. In many areas of computer science, including data structures, graph algorithms, parallel and distributed computing, and communication networks, network representations are crucial. Global representations characterize traditional networks in most cases. That is, one access a global data structure that represents the entire network in order to obtain relevant information. From social and communication networks to the Web, ma: graphs are present everywhere. These data sets' geometric depiction of the imposed network structure is a potent tool for aiding in data visualization and compreh Every graph considered here is finite, simple, undirected, connected, and non-trivial. The edge set $E=E(G)$ and vertex set $V=V(G)$ of the graph G , respectively. The ord graph was determined by the number of V elements, represented by the symbol $|V|$, while the size of the graph was determined by the number of E elements, indic the symbol $|E|$. The terms and notation used here are from J.A. Bondy and U.S.R. Murthy [2]. Roger Entringer suggested the idea of prime labelling, which was then in a study by us [20]. When the largest common divisor of two numbers a and b is 1, then pair is said to be relatively prime. Prime graphs have been extensively res The path P_n on n vertices is a prime graph, according to Fu. H[4]. All trees have prime labelling, according to Roger Entringer's hypothesis from around 1980, which been proven yet. S. K. Vaidhya and K. K. Kanmani have demonstrated that the graphs obtained by identifying any two vertices, duplicating an arbitrary vertex, and s any vertex in a cvcle admit prime labelling. The graph obtained by duplicating all the vertices of a graph is known as duplication of the graph in [22]

[View Application Status](#)

[Terms & conditions \(https://ipindia.gov.in/Home/Termsconditions\)](https://ipindia.gov.in/Home/Termsconditions) [Privacy Policy \(https://ipindia.gov.in/Home/Privacypolicy\)](https://ipindia.gov.in/Home/Privacypolicy)

[Copyright \(https://ipindia.gov.in/Home/copyright\)](https://ipindia.gov.in/Home/copyright) [Hyperlinking Policy \(https://ipindia.gov.in/Home/hyperlinkingpolicy\)](https://ipindia.gov.in/Home/hyperlinkingpolicy)

[Accessibility \(https://ipindia.gov.in/Home/accessibility\)](https://ipindia.gov.in/Home/accessibility) [Contact Us \(https://ipindia.gov.in/Home/contactus\)](https://ipindia.gov.in/Home/contactus) [Help \(https://ipindia.gov.in/Home/help\)](https://ipindia.gov.in/Home/help)

Content Owned, updated and maintained by Intellectual Property India, All Rights Reserved.

Page last updated on: 26/06/2019